46. (New) A process for producing a semiconductor integrated circuit device according to claim 24, wherein the floating gates are formed as self-aligned to the third gates.

REMARKS

Claims 9, 10, 24, 32, and 33 have been amended to eliminate the improper multiple dependencies. Claims 40-46 correspond to the dependencies eliminated from the amended claims.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

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9. (Amended) A process according to any one of Claims [1 to 8] 1-5, 7, or 8, wherein the third gates are self-aligned to the floating gates.

10. (Amended) A process according to any one of Claims [1 to 8] 1-5, 7, or 8, wherein the floating gates are self-aligned to the third gates.

24. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims [19 to 23] 19-21 or 23, wherein the polycrystalline silicon film has a film thickness thinner than that of the first pattern which becomes the floating gates.

32. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims [14 to 31] 14-21, 23, or 25-31, wherein the third gates are formed as self-aligned to the floating gates.

33. (Amended) A process for producing a semiconductor integrated circuit device according to any one of claims [14 to 31] 14-21, 23, or 25-31, wherein the floating gates are formed as self-aligned to the third gates.